doppioDB – A Hardware Accelerated Database

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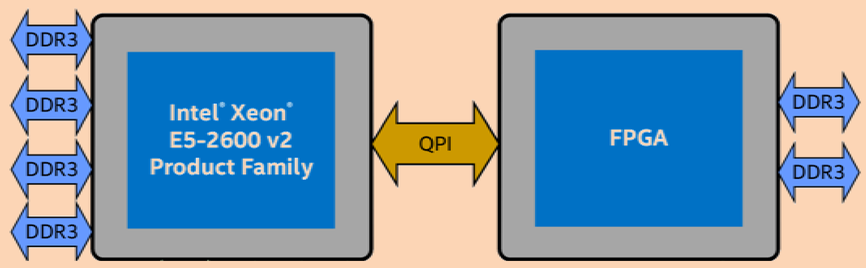
Emerging new platforms

Hybrid CPU-FPGA Architectures:
- Programmable hardware
- Direct access to shared memory
- FPGA as co-processor (instead of accelerator)

No need for data partitioning, copy or reformatting

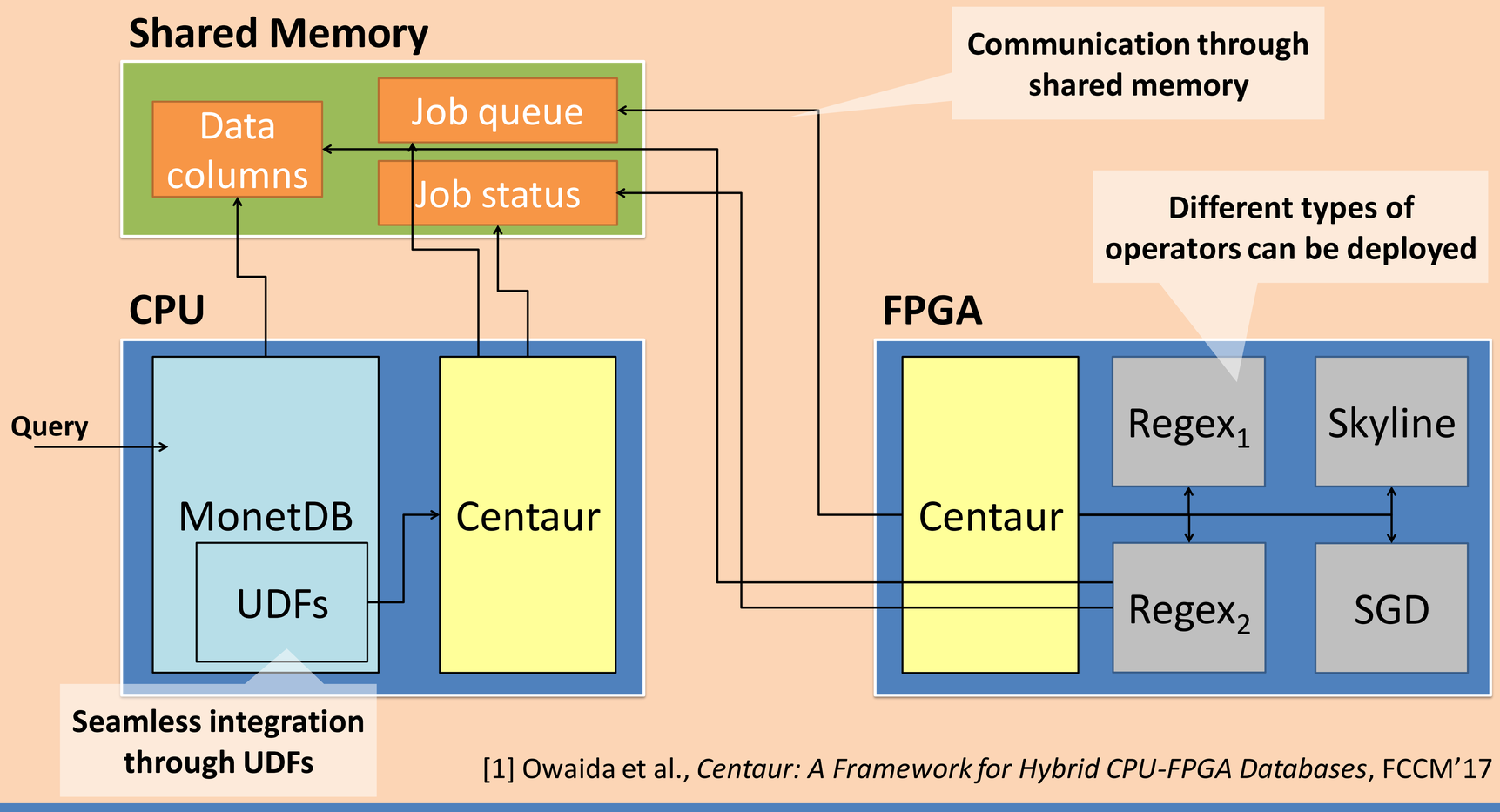
Intel Xeon+FPGA (v1)



DATABASE OF THE FUTURE

Hybrid database

Integration:
- UDFs can create and monitor jobs on the FPGA through Centaur[1]
- Operators on the FPGA are represented as hardware threads
- Concurrent execution of hardware operators

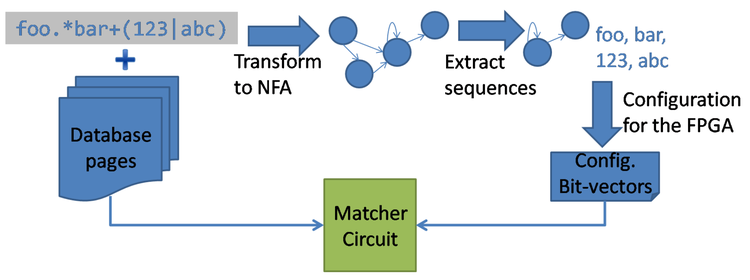


[1] Owaida et al., *Centaur: A Framework for Hybrid CPU-FPGA Databases*, FCCM'17

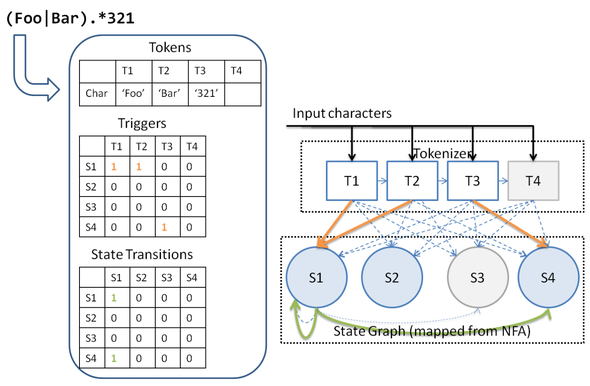
Hardware operators

Compute Intensive

Regular Expression [2]

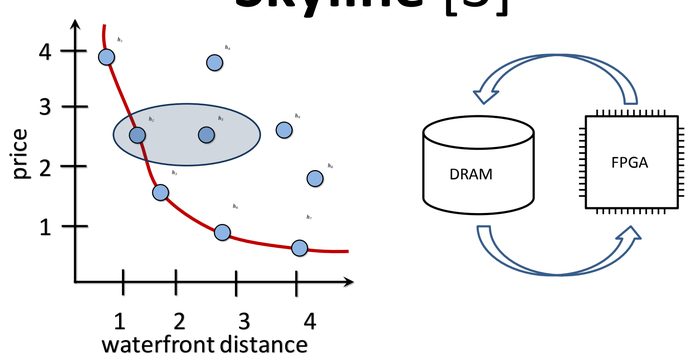


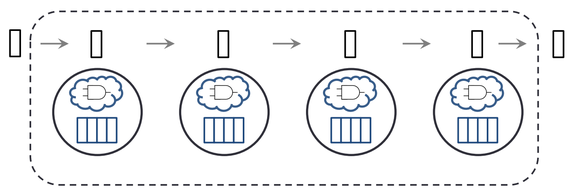
- NFA skeleton parameterized at run-time
- Expression translated into config. vector
- High throughput by deploying parallel NFAs



Deep Pipelining

Skyline [3]

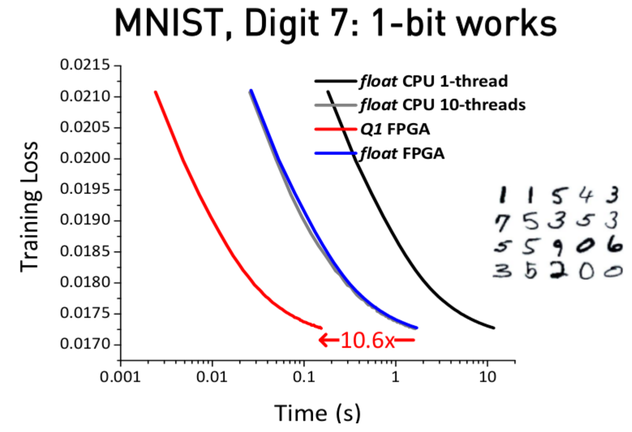




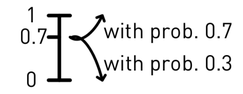
- Keeps candidate set in on-chip pipeline composed of memory cells and comparison logic
- Depending on result size performs multiple iterations

Custom precision

SGD [4]



- Works on compressed data (Probabilistic rounding to <32 bits)



=> More computation per data moved
- Exploits MIMD parallelism
- Implements custom data types

[2] Sidler et al., *Accelerating Pattern Matching Queries in Hybrid CPU-FPGA Architectures*, SIGMOD'17
[3] Woods et al., *Parallel Computation of Skyline Queries*, FCCM'13
[4] Kara et al., *FPGA accelerated Dense Linear Machine Learning: A Precision-Convergence Trade-off*, FCCM'17

Acknowledgements: We would like to thank Intel for their generous donation of the HARP v1 prototype.
This work is funded in part through the Microsoft Joint Research Center MSR-ETHZ-EPFL.

systems.ethz.ch/fpga
github.com/fpgasystems