**Emerging new platforms**

Hybrid CPU-FPGA Architectures:
- Programmable hardware
- Direct access to shared memory
- FPGA as co-processor (instead of accelerator)

**Hybrid database**

Integration:
- UDFs can create and monitor jobs on the FPGA through Centaur[1]
- Operators on the FPGA are represented as hardware threads
- Concurrent execution of hardware operators

**Hardware operators**

**Regular Expression [2]**
- NFA skeleton parameterized at run-time
- Expression translated into config. vector
- High throughput by deploying parallel NFAs

**Deep Pipelining**
- Keeps candidate set in on-chip pipeline composed of memory cells and comparison logic
- Depending on result size performs multiple iterations

**Custom precision**
- Works on compressed data (Probabilistic rounding to <32 bits)
- Exploits MIMD parallelism
- Implements custom data types

**Database of the future**

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[1] Owaida et al., Centaur: A Framework for Hybrid CPU-FPGA Databases, FCCM’17

[2] Sidler et al., Accelerating Pattern Matching Queries in Hybrid CPU-FPGA Architectures, SIGMOD’17
